IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	**Jason GOSIOR et al.**
Serial No.:	09/843,178
Filing Date:	04/26/2001
Title:	**MULTITHREAD EMBEDDED PROCESSOR WITH INPUT/OUTPUT CAPABILITY**
Group Art Unit:	2183
Examiner:	Li, Aimee J.

DECLARATION UNDER 37 C.F.R. § 1.132

TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I, Jason J. Gosior, of St. Albert, Alberta, Canada, hereby declare as follows:

1. I am one of the named co-inventors in respect of U.S. Patent Application No. 09/843,178 ("USPA 09/843,178"), and I am also an employee of the Assignee, Eleven Engineering Incorporated ("EEI"). As such, I have personal knowledge of all matters deposed to herein, except where based on information and belief, and where so stated I verily believe same to be true. All statements made by me in this Declaration are made with the knowledge that willful false statements are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of USPA 09/843,178 and any patent that may issue therefrom.

2. I received an Honors Diploma in Electronics Engineering Technology from the Northern Alberta Institute of Technology (Edmonton, Alberta) in 1994. I received a Bachelor of Science Degree in Electrical Engineering from the University of Alberta (Edmonton, Alberta) in 1997. I am registered as a Professional Engineer with the Association of Professional Engineers, Geologists and Geophysicists of Alberta (APEGGA).

3. I have been employed by EEI since my graduation from the University of Alberta in 1997. I have held the position of Manager, Hardware R & D, from June 2002 to the present.

4. I have reviewed and am thoroughly familiar with the Final Action issued by the USPTO on May 4, 2006 in connection with USPA 09/843,178, along with all references cited therein. I make this Declaration to provide evidence of commercial success of the invention claimed in USPA 09/843,178, in support of the Applicants' traversal of the claim rejections set out in the Final Action on grounds of obviousness under 35 U.S.C. § 103.

5. EEI has achieved commercial success creating RF (Radio Frequency) communication solutions using multithreading architectures in accordance with Claim 1 as currently of record in USPA 09/843,178. EEI sells processors using this architecture under the names "XInC"™ and "XInC2"™; accordingly, references herein to "XInC" products may be understood as referring to processors having architectures corresponding to the claimed invention.

6. EEI started selling microcontrollers using the XInC architecture in April 2002. Since then, EEI has shipped a total of 865,908 XInC microcontrollers, and currently has 113,000 in production. The majority of the XInC microcontrollers sold by EEI to date have been sold to customers for incorporation into DWA (Digital Wireless Audio) products. However, some customers have used the XInC microcontroller in wireless Ethernet links. These two applications are similar in the important sense that they transmit real-time data over an RF link.

7. Presented below is a list of customers who have purchased XInC microcontrollers from EEI to date, along with names or descriptions of products into which these customers have incorporated XInC microcontrollers:

- Acoustic Research 2.4GHz headphones
- Acoustic Research 2.4GHz flat panel speakers
- Acoustic Research 2.4GHz tower speakers
- Acoustic Research 2.4GHz amplifier block
- Acoustic Research 2.4GHz outdoor speaker
- Airus Airsurround
- AvaLAN 900 MHz Wireless Ethernet
- Bose SL2 wireless adapter for Lifestyle and Acoustimass home theatre systems
- Canton CD-3500 wireless speakers
- Logitech Play Link (wireless Ethernet link)
- Logitech z-5450 speakers

- Maxstream 900 MHz Wireless Ethernet
- Nyko Wireless Net Extender (wireless Ethernet link)
- Oregon Scientific iBall
- Oregon Scientific Sphere
- Promowide headphones
- Samsung 2.4GHz headphones
- SoundCast audioCast
- SoundCast iCast
- Teufel Home Theatre Rear Speakers

8. In cases where XInC microcontrollers were purchased for incorporation into DWA products, the XInC microcontrollers were provided in conjunction with EEI's "Squeak"™ DWA system. The XInC microcontroller is in fact the primary component of the "Squeak" system.

9. EEI has been advised by several customers chose the "Squeak" system for their DWA products because it had been found to provide the best quality of service ("QoS"). QoS is a term of art in the field of wireless audio, and it refers to reliability of data signal transmission. In wireless audio systems, good QoS is very important and very difficult to achieve, since what is being transported is a real-time signal. Real-time signals are fleeting, and therefore the transmit node cannot take whatever time is required to transmit the data; the data must be transferred as a stream to the receive node. Any break in this data stream will result in dropouts or "crackles" or "pops" in the resulting audio -- i.e., poor QoS. A reliable data stream with no discontinuities is considered good QoS. QoS may be measured quantitatively by placing the wireless system at a fixed range in a predetermined environment and measuring mean time between discontinuities.

10. EEI has been advised by several of its customers that they decided to purchase EEI's XInC microcontrollers on the basis of their own QoS testing programs in which the XInC/Squeak system was tested, along with competitors' systems, in the presence of interfering 2.4 GHz devices. Invariably, the XInC/Squeak solution exhibited the best QoS performance.

11. I am informed by Mr. Mike Szelewicki (EEI's Manager, Field Applications Engineering) that he has been advised by numerous customers regarding comparative tests that they performed and in which EEI's Squeak DWA system out-performed the tested competitor systems in terms of QoS. Presented below is a list of customers who have provided such information to Mr.

Szalewicki regarding QoS testing, along with references to specific competitor systems against which they tested the Squeak system:

Airus:	SQUEAK 1.5 vs. Bluetooth & Syncomm
Audio Vox:	SQUEAK 1.5 vs. STS
Bose, USA:	SQUEAK 1.5 vs. Bluetooth
Canton, Germany:	SQUEAK 1.5 vs. STS and Syncomm
Cobalt Industrial:	SQUEAK 1.5 vs. Syncomm
Creative Labs:	SQUEAK 1.5 vs. Syncomm
Foster, Japan:	SQUEAK 1C vs. Kleer and Syncomm
Gamma:	SQUEAK 1.5 vs. Syncomm
Gold Peak, HK:	SQUEAK 1.5 vs. Syncomm
Innovation:	SQUEAK 1.5 vs. Bluetooth
Jazz Speaker, Taiwan:	SQUEAK 1.5 vs. Syncomm
LG, Korea:	SQUEAK 1.5 vs. Syncomm
Meiloon, Taiwan:	SQUEAK 1.5 vs. Bluetooth
Saitek:	SQUEAK 1.5 vs. Bluetooth
Sony, Malaysia:	SQUEAK 1C vs. Bluetooth and Syncomm
Symprotech Corp.:	SQUEAK 1.5 vs. Bluetooth
Uniden, Japan:	SQUEAK 1.5 vs. Bluetooth

12. At the heart of EEI's Squeak DWA system is a microcontroller that uses the XInC multithreading architecture in accordance with the invention as currently claimed in USPA 09/843,178. It is this architecture that allows us to write the Squeak protocol and achieve higher QoS than competitor systems, while keeping the processor clock rate low, and processor cost to a minimum.

13. The key to providing good QoS is to provide the maximum retransmission margin. Every digital audio system adds latency to the audio stream. For most applications this is minimized, typically to be less than 30 ms. Any time that is spent by XInC processing the audio, either compressing or packetizing, is subtracted from the overall system latency of 30 ms. Thus the available time for retransmission is reduced. The DWA systems that use Squeak typically have a processing latency of 2.5 ms. This allows 27.5 ms for retransmission over the RF link.

14. XInC achieves the 2.5 ms of processing latency by dividing the whole firmware task across 7 threads. The thread tasks are written in such a way that their processing loops operate independently from each other. Therefore each loop has a predictable processing time that will never change. The processing time is balanced across the threads to minimize the overall latency. This may be further understood with reference to the attached **Appendix A**, which is a diagram of the Squeak firmware. The data flow is arranged in a pipeline, where each stage processes a portion of audio, then hand it off to the next stage. The stages all process data at the same time, such that when the first portion of audio is completed and moved to the next stage, the next portion is immediately processed. There is no processing overhead required to move the data between the threads.

15. Most of the processing time (approximately 95%) is spent in threads T2 to T6. One example implementation using a conventional serial processor (see **Appendix B**) would be to put the processing tasks in T2 and T6 in a large loop. T1 and T7 would be serviced on an interrupt basis. This would require a much higher clock rate for the serial processor. The three main reasons for the higher clock rate are as follows:

(a) Each time the processor switches between the processing tasks, there would be a context switch. This introduces extra instructions that would have to be executed.

(b) 95% of the processing task would have to be completed faster compared to XInC. This is because the input/output tasks (T1 and T7) will cause interrupts, to move the streaming audio data inform the audio source and out to the RF. These interrupts necessitate the use of context switches; these context switches represent additional processing overhead that is not present in the XInC architecture.

(c) In order to create a reliable system using a serial processor as in Appendix B, margin would have to be added to ensure that tasks T2 to T6 can be completed in time, given the peak interrupt rate required by T1 and T7.

16. With particular reference to the microprocessor described in U.S. Patent No. 5,933,627 (Parady), cited in the Final Action dated May 4, 2006, an increased clock rate would still be required to meet the latency margin of the Squeak system. The processor described in Parady is

still fundamentally a serial processor that has been enhanced to accelerate the speed of processing a single series of instructions, or multiple threads assuming that the same functional unit is not required at the same time. While the system is running, collisions may still occur, and cannot be predicted (a collision in this sense is where two instructions require the same functional unit at the same time, requiring the dispatch unit to choose the instruction from one thread, and delay the other). The processing speed must then be increased to add margin, and ensure that tasks T2 to T6 are completed in time. It can be seen from Appendix A that these inherent drawbacks of conventional serial processors and the Parady processor are absent from the XInC processor.

17. In summary, the information set out in paragraphs 12-16 above, read in conjunction with Appendices A and B, clearly illustrates and explains how EEI's XInC processor achieves higher QoS than competitor processors, as a direct result of the use of novel processor architecture in accordance with the invention claimed in USPA 09/843,178.

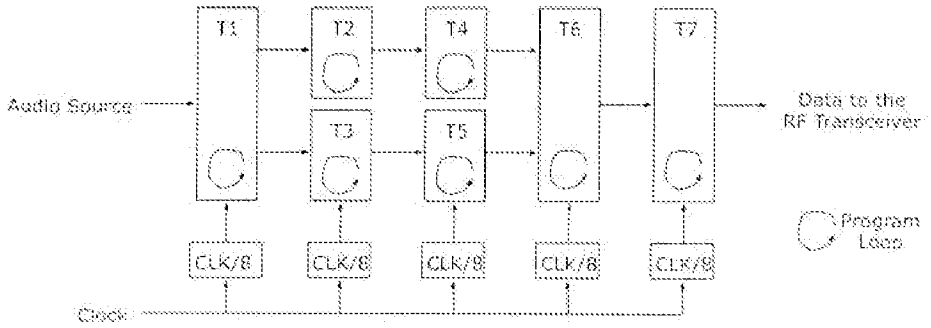
Signed at Edmonton, Alberta, and
respectfully submitted by:

Witness

JASON J. GOSIOR
November 5, 2006

Attachments:
Appendix A: Data Flow Diagram – Squeak DWA system [1 page]
Appendix B: Data Flow Diagram – serial processor [1 page]

Appendix A
Data Flow Diagram for Squeak DWA System



Appendix B
Data Flow Diagram for Serial Processor